

## MM1702A 2048-Bit (256 × 8) UV Erasable PROM

### General Description

The MM1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The MM1702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The MM1702AQ is packaged in a 24-pin dual-in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The MM1702AD is packaged in a 24-pin dual-in-line package with a metal lid and is not erasable.

The circuitry of the MM1702A is entirely static; no clocks are required.

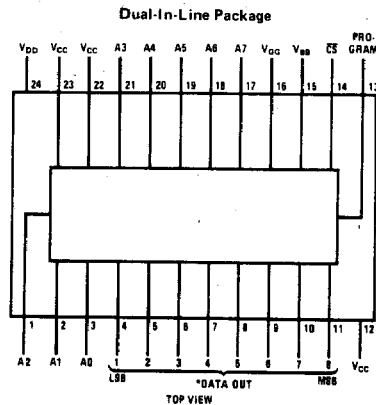
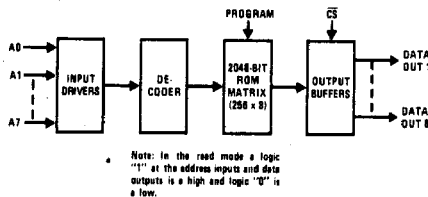
A pin-for-pin metal mask programmed ROM, the MM1302 is ideal for large volume production runs of systems initially using the MM1702A.

The MM1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

### Features

- Fast programming—30 seconds for all 2048 bits
- All 2048 bits guaranteed programmable—100% factory tested
- Fully decoded, 256 × 8 organization
- Static MOS—no clocks required
- Inputs and outputs DTL and TTL compatible
- TRI-STATE® output—OR-tie capability
- Simple memory expansion—chip select input lead
- Direct replacement for the Intel 1702A

### Block and Connection Diagrams



\*This pin is the data input lead during programming.

Order Number MM1702AQ  
See NS Package J24CQ

#### Pin Names

A0-A7	Address Inputs
CS	Chip Select Input
D <sub>OUT 1</sub> - D <sub>OUT 8</sub>	Data Outputs

#### Pin Connections\*

MODE/PIN	12 (V <sub>CC</sub> )	13 (PROGRAM)	14 (CS)	15 (V <sub>BB</sub> )	16 (V <sub>GG</sub> )	22 (V <sub>CC</sub> )	23 (V <sub>CC</sub> )
Read	V <sub>CC</sub>	V <sub>CC</sub>	GND	V <sub>CC</sub>	V <sub>GG</sub>	V <sub>CC</sub>	V <sub>CC</sub>
Programming	GND	Program Pulse	GND	V <sub>BB</sub>	Pulsed V <sub>GG</sub> (V <sub>ILAP</sub> )	GND	GND

\*The external lead connections to the MM1702A differ, depending on whether the device is being programmed or used in read mode. (See following table.) In the programming mode, the data inputs are pins 4-11 respectively.

## Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +125°C
Power Dissipation	2W
Read Operation	
Input Voltages and Supply Voltages with Respect to $V_{CC}$	+0.5V to -20V
Program Operation	
Input Voltages and Supply Voltages with Respect to $V_{CC}$	-48V
Lead Temperature (Soldering, 10 seconds)	300°C

## Read Operation DC Characteristics

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5V \pm 5\%$ ,  $V_{DD} = -9V \pm 5\%$ ,  $V_{GG} = -9V \pm 5\%$ , unless otherwise noted. Typical values are at nominal voltages and  $T_A = 25^\circ\text{C}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{LI}$	Address and Chip Select Input Load Current	$V_{IN} = 0.0V$			1	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0.0V$ , $\overline{CS} = V_{CC} - 2$			1	$\mu\text{A}$
$I_{DD0}$	Power Supply Current	$V_{GG} = V_{CC}$ , $\overline{CS} = V_{CC} - 2$ $I_{OL} = 0.0\text{ mA}$ , $T_A = 25^\circ\text{C}$ , (Note 2)		5	10	mA
$I_{DD1}$	Power Supply Current	$\overline{CS} = V_{CC} - 2$ , $I_{OL} = 0.0\text{ mA}$ , $T_A = 25^\circ\text{C}$		35	50	mA
$I_{DD2}$	Power Supply Current	$\overline{CS} = 0.0$ , $I_{OL} = 0.0\text{ mA}$ , $T_A = 25^\circ\text{C}$		32	46	mA
$I_{DD3}$	Power Supply Current	$\overline{CS} = V_{CC} - 2$ , $I_{OL} = 0.0\text{ mA}$ , $T_A = 0^\circ\text{C}$		38.5	60	mA
$I_{CF1}$	Output Clamp Current	$V_{OUT} = -1.0V$ , $T_A = 0^\circ\text{C}$		8	14	mA
$I_{CF2}$	Output Clamp Current	$V_{OUT} = -1.0$ , $T_A = 25^\circ\text{C}$			13	mA
$I_{GG}$	Gate Supply Current				1	$\mu\text{A}$
$V_{IL1}$	Input Low Voltage for TTL Interface		-1.0		$V_{CC} - 4.1$	V
$V_{IL2}$	Input Low Voltage for MOS Interface		$V_{DD}$		$V_{CC} - 6$	V
$V_{IH}$	Address and Chip Select Input High Voltage		$V_{CC} - 2$		$V_{CC} + 0.3$	V
$I_{OL}$	Output Sink Current	$V_{OUT} = 0.45V$	1.6	4		mA
$I_{OH}$	Output Source Current	$V_{OUT} = 0.0V$	-2.0			mA
$V_{DL}$	Output Low Voltage	$I_{OL} = 1.6\text{ mA}$		-0.7	0.45	V
$V_{OH}$	Output High Voltage	$I_{OH} = -100\mu\text{A}$	3.5	4.5		V

**Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Note 2:** Power-Down Option:  $V_{GG}$  may be clocked to reduce power dissipation. The average  $I_{DD}$  will vary between  $I_{DD0}$  and  $I_{DD1}$  depending on the  $V_{GG}$  duty cycle (see typical characteristics). For this option, please specify MM1702AL.

### Read Operation AC Characteristics

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{DD} = -9\text{V} \pm 5\%$ ,  $V_{GG} = -9\text{V} \pm 5\%$ , unless otherwise noted.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Freq.	Repetition Rate			1	MHz
$t_{OH}$	Previous Read Data Valid			100	ns
$t_{ACC}$	Address to Output Delay		0.7	1	$\mu\text{s}$
$t_{DVGG}$	Clocked $V_{GG}$ Set-Up (Note 1)	1			$\mu\text{s}$
$t_{CS}$	Chip Select Delay			100	ns
$t_{CO}$	Output Delay From $\overline{CS}$			900	ns
$t_{OD}$	Output Deselect			300	ns
$t_{OHC}$	Data Out Hold in Clocked $V_{GG}$ Mode (Note 1)			5	$\mu\text{s}$

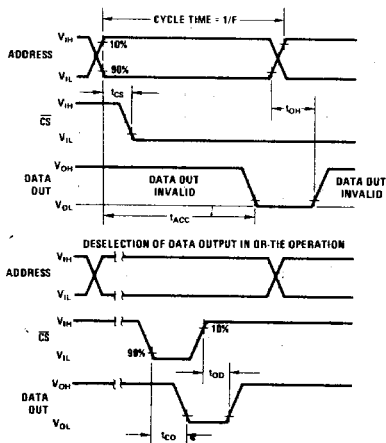
### Capacitance Characteristics $T_A = 25^\circ\text{C}$ (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$C_{IN}$	Input Capacitance	All Unused $V_{IN} = V_{CC}$		8	15	pF
$C_{OUT}$	Output Capacitance	Pins Are $\overline{CS} = V_{CC}$		10	15	pF
$C_{VGG}$	$V_{GG}$ Capacitance (Note 1)	At ac $V_{OUT} = V_{CC}$ Ground $V_{GG} = V_{CC}$			30	pF

Note 3: This parameter is periodically sampled and is not 100% tested.

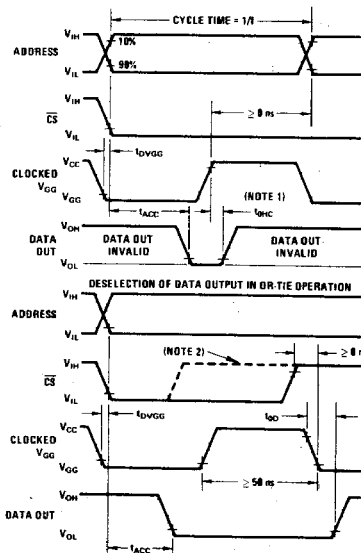
### Read Operation Switching Time Waveforms

(a) Constant  $V_{GG}$  Operation



Conditions of Test:  
Input pulse amplitude: 0-4V,  $t_r, t_f \leq 50$  ns. Output load is 1 TTL gate; measurements made at output of TTL gate ( $V_{OL} \leq 15$  mV,  $C_L = 15$  pF).

(b) Power-Down Option (Note 1)



Note 1: The output will remain valid for  $t_{OHC}$  as long as clocked  $V_{GG}$  is at  $V_{CC}$ . An address change may occur as soon as the output is sensed (clocked  $V_{GG}$  may still be at  $V_{CC}$ ). Data becomes invalid for the old address when clocked  $V_{GG}$  is returned to  $V_{GG}$ .

Note 2: If  $\overline{CS}$  makes a transition from  $V_{OL}$  to  $V_{OH}$  while clocked  $V_{GG}$  is at  $V_{CC}$ , then deselection of output occurs at  $t_{OD}$  as shown in static operation with constant  $V_{GG}$ .

## Programming Operation DC Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = 0\text{V}$ ,  $V_{BB} = 12\text{V} \pm 10\%$ ,  $\overline{CS} = 0\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{L11P}$	Address and Data Input Load Current	$V_{IN} = -48\text{V}$			10	mA
$I_{L12P}$	Program and $V_{GG}$ Load Current	$V_{IN} = -48\text{V}$			10	mA
$I_{BB}$	$V_{BB}$ Supply Load Current	(Note 5)		10	100	mA
$I_{DDP}$	Peak $I_{DD}$ Supply Load Current	$V_{DD} = V_{PROG} = -48\text{V}$ $V_{GG} = -35\text{V}$ (Note 4)		200	300	mA
$V_{IHP}$	Input High Voltage				0.3	V
$V_{IL1P}$	Pulsed Data Input Low Voltage		-46		-48	V
$V_{IL2P}$	Address Input Low Voltage		-40		-48	V
$V_{IL3P}$	Pulsed Input Low $V_{DD}$ and Program Voltage		-46		-48	V
$V_{IL4P}$	Pulsed Input Low $V_{GG}$ Voltage		-35		-40	V

Note 4:  $I_{DDP}$  flows only during  $V_{DD}$ ,  $V_{GG}$  on time.  $I_{DDP}$  should not be allowed to exceed 300 mA for greater than 100 $\mu\text{s}$ . Average power supply current  $I_{DDP}$  is typically 40 mA at 20% duty cycle.

Note 5: The  $V_{BB}$  supply must be limited to 100 mA max current to prevent damage to the device.

## Programming Operation AC Characteristics

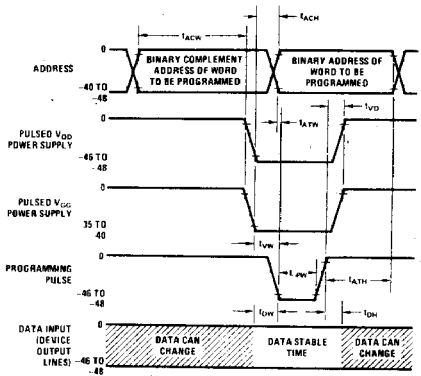
$T_A = 25^\circ\text{C}$ ,  $V_{CC} = 0\text{V}$ ,  $V_{BB} = 12\text{V} \pm 10\%$ ,  $\overline{CS} = 0\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Duty Cycle ( $V_{DD}$ , $V_{GG}$ )				20	%
$t_{\phi PW}$	Program Pulse Width	$V_{GG} = -35\text{V}$ , $V_{DD} = V_{PROG} = -48\text{V}$			3	ms
$t_{DW}$	Data Set-Up Time		25			$\mu\text{s}$
$t_{DH}$	Data Hold Time		10			$\mu\text{s}$
$t_{VW}$	$V_{DD}$ , $V_{GG}$ Set-Up		100			$\mu\text{s}$
$t_{VD}$	$V_{DD}$ , $V_{GG}$ Hold		10		100	$\mu\text{s}$
$t_{ACW}$	Address Complement Set-Up	(Note 6)	25			$\mu\text{s}$
$t_{ACH}$	Address Complement Hold	(Note 6)	25			$\mu\text{s}$
$t_{ATW}$	Address True Set-Up		10			$\mu\text{s}$
$t_{ATH}$	Address True Hold		10			$\mu\text{s}$

Note 6: All 8 address bits must be in the complement state when pulsed  $V_{DD}$  and  $V_{GG}$  move to their negative levels. The addresses (0-255) must be programmed as shown in the timing diagram until data reads true, then over-programmed 4 times that amount. (Symbolized by  $x + 4x$ .)

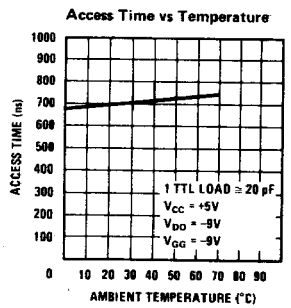
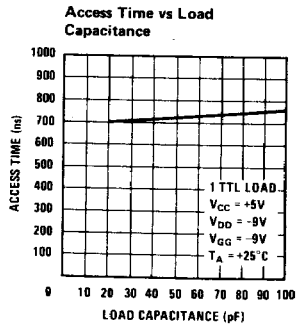
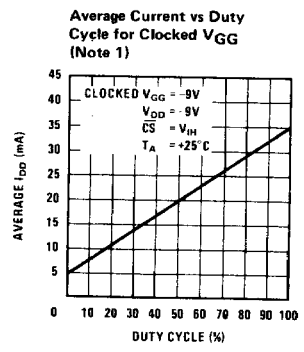
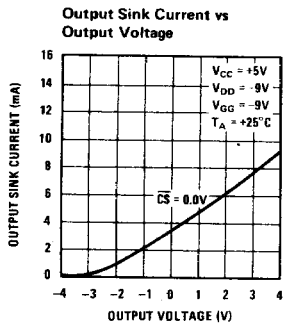
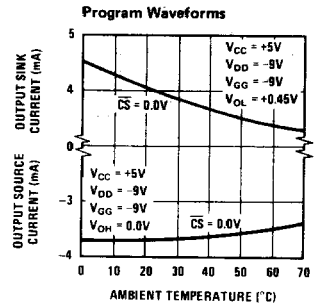
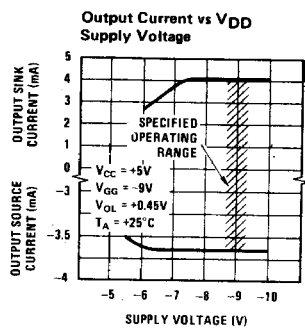
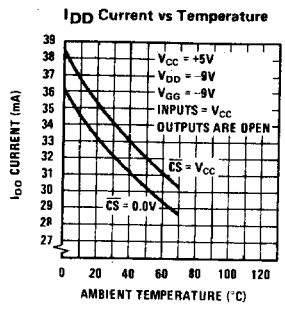
# Programming Operation Switching Time Waveforms

MM1702A



Conditions of Test:  
Input pulse rise and fall times = 1 ns  
 $CS = 0V$

## Typical Performance Characteristics



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## Operation of the MM1702A in Program Mode

Initially, all 2048 bits of the ROM are in the "0" state (output low). Information is introduced by selectively programming "1's" (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode (see table for logic levels). All 8 address bits must be in the binary complement state when pulsed  $V_{DD}$  and  $V_{GG}$  move to their negative levels. The addresses must be held in their binary complement state for a minimum of  $25\mu\text{s}$  after  $V_{DD}$  and  $V_{GG}$  have moved to their negative levels. The addresses must then make the transition to their true state a

minimum of  $10\mu\text{s}$  before the program pulse is applied. The addresses should be programmed in the sequence 0-255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level ( $-48\text{V}$ ) will program a "1" and a high data input level (ground) will leave a "0" (see table on page 4-4). All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the programming,  $V_{GG}$ ,  $V_{DD}$  and the Program Pulse are pulsed signals.

## MM1702A Erasing Procedure

The MM1702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of  $2537\text{\AA}$ . The recommended integrated dose (i.e., UV intensity x exposure time) is  $6\text{W sec/cm}^2$ . Examples of ultraviolet sources which can erase the MM1702A in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used with-

out short-wave filters, and the MM1702A to be erased should be placed about one inch away from the lamp tubes. There exists no absolute rule for erase time. Establish a worst case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. (May be expressed as  $x + 2x$ .)