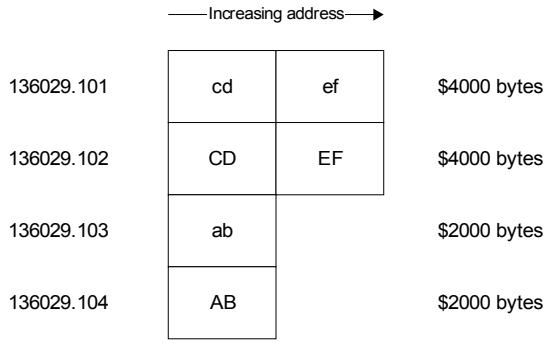
I, Robot shared CPU & Mathbox RAM

(For the time being) you can reach me at lordfrito@comcast.net or john.manfreda@idselectronics.com)

Layout of mathbox ROMs

The following diagram shows the 4 mathbox ROMs, and the 6 banks ($2000 bytes each) contained inside these ROMs.



The data stored in these ROMs is 16-bit. Each ROM stores either the high byte of a bank, or the low byte. Banks desginated with **uppercase** letters are high data, banks designated with **lowercase** letters are low data.

Mathbox address space:

The mathbox addresses 16-bit data mapped from $0000 to $6FFF. The mathbox memory map is the following.

WORD address	Data
$0000 - $0FFF	2K RAM shared between mathbox and CPU
$1000 - $1FFF	Aa
$2000 - $2FFF	Bb
$3000 - $3FFF	Cc
$4000 - $4FFF	Dd
$5000 - $5FFF	Ee
$6000 - $6FFF	Ff

Please note that this memory map does not show video accelerator RAM which is accessible by the mathbox.

CPU address space:

The CPU addresses 7 banks of 8-bit data. Each bank is mapped in the CPU address space from $2000 to $3FFF. These banks are the following:

BYTE address	Bank	Data
$2000 - $3FFF	1	2K RAM shared between mathbox and CPU
$2000 - $3FFF	2	Aa
$2000 - $3FFF	3	Bb
$2000 - $3FFF	4	Cc
$2000 - $3FFF	5	Dd
$2000 - $3FFF	6	Ee
$2000 - $3FFF	7	Ff

Please note that there are 2 additional banks of data from $2000 to $3FFF, which are the video accelerator RAM.

Bank switching is controlled by register $1180. The following table is used to decode the CPU bank switch register:

OUT4 (bit 4)	OUT3 (bit 3)	MPAGE2 (bit 2)	MPAGE1 (bit 1)	Bank
1	1	d/c	d/c	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7